WHAT IS CLAIMED IS:

1. A frequency/signal converter receiving an input clock signal and generating an output signal at an output terminal, said converter comprising:

a first circuit receiving the input clock signal and generating first and second logic signals that are complementary with one another;

a loop circuit that includes a first circuit line and a second circuit line that are each coupled between a first supply voltage and a second supply voltage, the first supply voltage being greater than the second supply voltage; and

an integrator device,

wherein a current proportional to the output signal of the converter flows in the loop circuit,

the first circuit line includes a first capacitive element, and a first switch for interrupting current flow into the first capacitive element, the first switch being controlled by the first logic signal,

the second circuit line includes a second capacitive element, and a second switch for interrupting current flow into the second capacitive element, the second switch being controlled by the second logic signal, and

the first and second circuit lines are alternatively coupled to an input terminal of the integrator device in order to obtain a substantially constant voltage signal at the input terminal of the integrator device, the integrator device providing the output signal of the converter.

2. The converter according to claim 1, wherein the first and second logic signals have a period that is twice the period of the input clock signal.

3. The converter according to claim 2, wherein the first and second logic signals each has a value of logic one for one half of its period and a value of logic zero for the other half of its period.

4. The converter according to claim 1, wherein the integrator device includes:

a transconductance operational amplifier, the amplifier receiving the substantially constant voltage signal at its inverting input terminal and a reference voltage at its non-inverting terminal; and

a third capacitive element,

wherein the amplifier provides a current signal that is integrated by the third capacitive element so as to produce the output signal of the converter.

5. The converter according to claim 1,

wherein the first circuit line further includes a third switch for discharging the first capacitive element, and

the second circuit line further includes a fourth switch for discharging the second capacitive element.

6. The converter according to claim 5, wherein the third and fourth switches are controlled by pulse signals that correspond to the rising edges of the first and second logic signals.

7. A switching regulator for providing a regulated voltage to a load that is coupled to an output terminal of the regulator, said regulator comprising:

a first transistor having a first terminal coupled to an input terminal and a second terminal coupled to the output terminal of the regulator;

at least one inductance coupled between the second terminal of the transistor and the output terminal of the regulator;

a first circuit coupled to the output terminal for providing a feedback signal that is representative of the regulated voltage;

a second circuit coupled to the inductance for providing a second signal that is representative of the current flowing through the inductance;

a control circuit coupled to the first and second circuits and the transistor, the control circuit receiving an input clock signal and driving the first transistor so as to interrupt a current flow from the input terminal to the output terminal according to a predetermined duty-cycle; and

a device receiving the input clock signal and generating a slope compensation signal that is proportional to the frequency of the input clock signal when the duty-cycle exceeds a predetermined value, the slope compensation signal being coupled to the control circuit.

8. The regulator according to claim 7, further comprising a comparator coupled to the first and second circuits, the comparator comparing a sum of the feedback signal and the slope compensation signal with the second signal, the output of the comparator being supplied to the control circuit.

9. The regulator according to claim 7, wherein the device is a frequency/signal converter comprising:

a first circuit receiving the input clock signal and generating first and second logic signals that are complementary with one another;

a loop circuit that includes a first circuit line and a second circuit line that are each coupled between a first supply voltage and a second supply voltage, the first supply voltage being greater than the second supply voltage; and

an integrator device,

wherein a current proportional to the output signal of the converter flows in the loop circuit,

the first circuit line includes a first capacitive element, and a first switch for interrupting current flow into the first capacitive element, the first switch being controlled by the first logic signal,

the second circuit line includes a second capacitive element, and a second switch for interrupting current flow into the second capacitive element, the second switch being controlled by the second logic signal, and

the first and second circuit lines are alternatively coupled to an input terminal of the integrator device in order to obtain a substantially constant voltage signal at the input terminal of the integrator device, the integrator device providing the output signal of the converter.

10. The regulator according to claim 9, wherein the first and second logic signals of the converter have a period that is twice the period of the input clock signal.

11. The regulator according to claim 10, wherein the first and second logic signals each has a value of logic one for one half of its period and a value of logic zero for the other half of its period.

12. The regulator according to claim 9, wherein the integrator device includes:

a transconductance operational amplifier, the amplifier receiving the substantially constant voltage signal at its inverting input terminal and a reference voltage at its non-inverting terminal; and

a third capacitive element,

wherein the amplifier provides a current signal that is integrated by the third capacitive element so as to produce the output signal of the converter.

13. The regulator according to claim 9,

wherein the first circuit line further includes a third switch for discharging the first capacitive element, and

the second circuit line further includes a fourth switch for discharging the second capacitive element.

14. The regulator according to claim 13, wherein the third and fourth switches are controlled by pulse signals that correspond to the rising edges of the first and second logic signals.

15. An integrated circuit including at least one frequency/signal converter that receives an input clock signal and generates an output signal at an output terminal, said converter comprising:

a first circuit receiving the input clock signal and generating first and second logic signals that are complementary with one another;

a loop circuit that includes a first circuit line and a second circuit line that are each coupled between a first supply voltage and a second supply voltage, the first supply voltage being greater than the second supply voltage; and

an integrator device,

wherein a current proportional to the output signal of the converter flows in the loop circuit,

the first circuit line includes a first capacitive element, and a first switch for interrupting current flow into the first capacitive element, the first switch being controlled by the first logic signal,

the second circuit line includes a second capacitive element, and a second switch for interrupting current flow into the second capacitive element, the second switch being controlled by the second logic signal, and

the first and second circuit lines are alternatively coupled to an input terminal of the integrator device in order to obtain a substantially constant voltage signal at the input terminal of the integrator device, the integrator device providing the output signal of the converter.

16. The integrated circuit according to claim 15, wherein the first and second logic signals have a period that is twice the period of the input clock signal.

17. The integrated circuit according to claim 16, wherein the first and second logic signals each has a value of logic one for one half of its period and a value of logic zero for the other half of its period.

18. The integrated circuit according to claim 15, wherein the integrator device includes:

a transconductance operational amplifier, the amplifier receiving the substantially constant voltage signal at its inverting input terminal and a reference voltage at its non-inverting terminal; and

a third capacitive element,

wherein the amplifier provides a current signal that is integrated by the third capacitive element so as to produce the output signal of the converter.

19. The integrated circuit according to claim 15,

wherein the first circuit line further includes a third switch for discharging the first capacitive element,

the second circuit line further includes a fourth switch for discharging the second capacitive element, and

the third and fourth switches are controlled by pulse signals that correspond to the rising edges of the first and second logic signals.